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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/696,018	10/29/2003	Satoru Adachi	TIJ-35055	7078

23494 7590 08/29/2006

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EXAMINER	
INGHAM, JOHN C	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 08/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/696,018	ADACHI, SATORU	
	Examiner	Art Unit	
	John C. Ingham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 July 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendments to the claims filed 3 July 2006 have been entered. The objection to claim 7 has been withdrawn.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims **1 and 2** are rejected under 35 U.S.C. 102(b) as being anticipated by Dierickx (US 2002/0022309).

4. Regarding claim **1**, Dierickx discloses in Fig 7 a solid-state image sensing device comprising an integration of plural pixels (¶02), which has a light-receiving portion that receives light and generates and accumulates a signal charge (¶37), and has the following parts: a semiconductor substrate (6) of the first electroconductive type (n type); a semiconductor layer (3) of the second electroconductive type (p type) that is formed on the principal surface of said semiconductor substrate; a gate electrode for pixel selection (120) formed via a gate insulating film on said semiconductor layer; a first semiconductor region (1) of the first electroconductive type (n) that is formed in the outer layer (3) in the light-receiving portion positioned on one side of (120); a second semiconductor region (4) of the first electroconductive type formed deeper than said first

region (1) in the outer layer of (43) in said light-receiving portion; and a third semiconductor region (2) of the first electroconductive type (n) formed in the outer layer of (3) on the other side of the gate electrode (120) for pixel selection, and containing an impurity (n type) and having an impurity concentration higher than that of said first region (1) (item 2 is doped n++, compared to items 1 and 4, doped n).

5. With regards to claim **2**, Dierickx discloses in Figure 7 the device of claim 1, wherein the structure of the device is capable of performing the intended use limitations of the claim 2 language. That is, the device of claim 1 receives and accumulates charge in the semiconductor layer (3) of the light-receiving portion, and is capable of forming a junction transistor with the semiconductor substrate (6), semiconductor layer (1), and second semiconductor region (4), wherein the modulation of the threshold voltage of this junction transistor is performed by the signal charge accumulation in the semiconductor layer. If a prior art structure is capable of performing the intended use as recited in the preamble, then it meets the claim. See, e.g., In re Schreiber, 128 F.3d 1473, 1477, 44 USPQ2d 1429, 1431 (Fed. Cir. 1997).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims **1-3** are rejected under 35 U.S.C. 103(a) as being unpatentable over Pan (US 6,287,886) and Dierickx.

8. Regarding claim **1**, Pan discloses in Figure 4 a solid-state image sensing device comprising a pixel (40), which has a light-receiving portion that receives light and generates and accumulates a signal charge, and has the following parts: a semiconductor substrate (42); a semiconductor region (43) of the second electroconductive type (p) that is formed on the principal surface of said semiconductor substrate; a gate electrode for pixel selection (48) formed via a gate insulating film on said semiconductor layer; a first semiconductor region (55) of the first electroconductive type (n) that is formed in the outer layer (43) in the light-receiving portion positioned on one side of (46); a second semiconductor region (50) of the first electroconductive type formed deeper than said first region (55) in the outer layer of (43) in said light-receiving portion; and a third semiconductor region (54) of the first electroconductive type (n) formed in the outer layer of (43) on the other side of the gate electrode (48) for pixel selection, and containing an impurity (n type) and having an impurity concentration higher than that of said first region (55) (item 55 is less than $10^{18}cm^{-3}$, item 54 is HDD, see col 3 ln 29, 41).

Pan does not disclose that the device (40) is part of an integration of plural pixels, nor does Pan specify that the substrate (42) be of the first electroconductive type (n type). Pan also does not disclose that the region (43) is a "layer", but instead specifies a well.

Dierickx teaches that substrates of either n or p type conductivity are used to make equivalent structures (nMOS or pMOS, ¶37). Dierickx also teaches (¶38) that a region may be equivalently formed by ion implantation (well) or epitaxial growth (layer). It would have been obvious to one of ordinary skill in the art at the time of the invention to use an n-type substrate rather than a p-type substrate, and a layer instead of a well as disclosed by Pan. Art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07. Finally, Dierickx teaches that it is well known to use pixels in an imaging array, and not singly (¶50), in order to fabricate an array of photodiodes into an integrated circuit. It would also have been obvious to integrate the single pixel disclosed into an array of plural pixels.

9. With regards to claim **2**, Pan discloses in Figure 4 the device of claim 1, wherein the structure of the device is capable of performing the functional limitations of the claim 2 language. That is, the device of claim 1 receives and accumulates charge in the semiconductor layer (p type 43) of the light-receiving portion, and is capable of forming a junction transistor with the semiconductor substrate (n type 42), semiconductor layer, and second semiconductor region (n type 50), wherein the modulation of the threshold voltage of this junction transistor is performed by the signal charge accumulation in the semiconductor layer. If a prior art structure is capable of performing the intended use as recited in the preamble, then it meets the claim. See, e.g., In re Schreiber, 128 F.3d 1473, 1477, 44 USPQ2d 1429, 1431 (Fed. Cir. 1997).

10. Regarding claim **3,** Pan discloses in column 1 line 16-17, the device of claim 1 further comprising: a gate electrode for reset (Fig 3 items 46) that is formed via gate

insulating film on said semiconductor layer, and a fourth semiconductor region (between two lower gates 46) of the second electroconductive type that is formed on the outer layer of said semiconductor layer on one side of said gate electrode for reset; said first semiconductor region (55) is formed in the outer layer of said semiconductor layer on the other side of said gate electrode for reset; said semiconductor layer, said gate electrode for reset, and said fourth semiconductor region form a buried channel type of transistor for reset (formed in layer 43), and said signal charge accumulated in said light-receiving portion is evacuated from said light-receiving portion when said transistor for reset operates (inherent function of a pixel reset transistor).

11. Claim **4** is rejected under 35 U.S.C. 103(a) as being unpatentable over Pan and Dierickx as applied to claim 3 above, and further in view of Guidash (US 6,466,266). Pan and Dierickx fail to specify wherein said gate electrode for pixel selection in one pixel is connected to said gate electrode for reset in the pixel adjacent to said one pixel.

Guidash teaches that sharing the signal lines may reduce signals within a sensor. Referring to Figure 6, the row select bus (37) of a pixel row previously read is employed as the reset gate bus (36) for the row currently being read. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Guidash on the device of Pan and Dierickx in order to reduce the total number of signal lines and hence the occlusion area (col 3 ln 56-57, and col 4 ln 1-3).

12. Claim **5** is rejected under 35 U.S.C. 103(a) as being unpatentable over Pan, Dierickx and Guidash as applied to claim 3 above, and further in view of Joo (US 6,121,115). Pan, Dierickx and Guidash do not specify a fifth semiconductor region of the first conductive type, having an impurity of the first conductive type (p) and having an impurity concentration higher than that of said first semiconductor region, formed in the outer layer of said semiconductor layer on the periphery of said first semiconductor region and in the portion other than the portion where said gate electrode for pixel selection and said gate electrode for reset are located.

Joo teaches a device having a channel stop impurity layer around the periphery of the device. The channel stop region has a higher impurity concentration than the substrate. It would have been obvious to one of ordinary skill in the art at the time of the invention to have included a fifth region in the periphery of the photodiode in order to improve device isolation (col 1 ln 23-25).

13. Claim **6** is rejected under 35 U.S.C. 103(a) as being unpatentable over Pan, Dierickx, Guidash, and Joo as applied to claim 5 above, and further in view of Kopley (US 2001/0024864). Pan, Dierickx, Guidash, and Joo do not specify a field plate formed as the gate electrode of a transistor for element separation, via a gate insulating film in the upper layer of the semiconductor layer between adjacent pixels on the outer periphery of said fifth semiconductor region.

Kopley teaches in Figure 6 a structure including a guard layer (40) over field edges of adjacent pixels, formed as a gate of a transistor via an insulating film (Fig 8

item 41). It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the field plate (40) along with the channel stop impurities as taught by Joo, in order to further isolate adjacent photodiodes (Kopley abstract).

14. Claims **7, 11, and 12** are rejected under 35 U.S.C. 103(a) as being unpatentable over Pan, Dierickx and Guidash as applied to claim 4 above, and further in view of Hashimoto (US 6,977,684).

15. Regarding claim **7**, Pan, Dierickx and Guidash disclose a solid-state image sensing device comprising each of the elements as discussed above in claims 1-4, including plural pixel rows formed from plural light-receiving elements arranged in a linear configuration (Guidash Fig 6), wherein each light-receiving element has the following parts: a semiconductor layer (Pan Fig 4 item 43) of a first conductive type formed on the principal surface of a semiconductor substrate (Pan Fig 4 item 42); and gate electrodes for read and reset of the facing light receiving elements in adjacent pixels electrically connected to each other (Guidash Fig 6).

Pan, Dierickx and Guidash do not disclose the rest of the limitations of claim 7, but Hashimoto teaches in Figure 14 light-receiving elements in each pixel row arranged offset by about ½ pitch from those in the adjacent rows to reduce moiré (col 12 ln 58); a gate electrode for read (Fig 3 item 40) formed via an insulating film on said semiconductor layer on one side of the pixel row; a gate electrode for reset (43) formed via an insulating film on said semiconductor layer on the other side of the pixel row; a first semiconductor region (32a) of the second conductive type formed in the region

between said gate electrodes for read and reset; a second semiconductor region of the second conductive type (below gate 36 of source-follower, see Fig 4), having an impurity concentration higher than that of said first semiconductor region and formed on said semiconductor layer in a region nearer said read gate electrode than said gate electrode for reset; a third semiconductor region (connected to item 37 in Fig 4) of the second conductive type, having an impurity concentration higher than that of said first semiconductor region and formed on said semiconductor layer in the region facing said first semiconductor region with said read gate (Fig 3 item 40) sandwiched between them; and a fourth semiconductor region (Fig 4, region left of reset gate 43) of the second conductive type, having an impurity concentration higher than that of said first semiconductor region in the region facing said first semiconductor region with said gate electrode for reset sandwiched between them.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Hashimoto regarding the ½ pitch offset of adjacent pixels, due to the correction of moiré (col 12 ln 58), and the rearrangement of regions is an obvious variation from those of the art. In re Kuhle, 526 F.2d 553, 188 USPQ 7 (CCPA 1975). MPEP 2144.04.

16. Regarding claim **11**, Hashimoto discloses a structure which can perform the intended use limitations of the claim, that is, when a first voltage is applied to said reset gate (Fig 4 item 43), the light-receiving element is reset and charge is evacuated, and when a voltage is applied to the read gate (Fig 3 item 40), a signal corresponding to the accumulated charge is output (onto bus 37). If a prior art structure is capable of

performing the intended use as recited in the preamble, then it meets the claim. See, e.g., In re Schreiber, 128 F.3d 1473, 1477, 44 USPQ2d 1429, 1431 (Fed. Cir. 1997).

17. With regards to claim **12**, an obvious variation of an n-channel imaging sensor is a p-channel sensor, as taught by Dierickx and applied to claim 1 above.

18. Claims **8, 13-15, and 18** are rejected under 35 U.S.C. 103(a) as being unpatentable over Pan, Dierickx, Guidash, and Hashimoto as applied to claim 7 above, and further in view of Ikeda (US 6,172,729). Joo and Kopley provide extra teachings regarding the field isolation regions.

19. Regarding claim **8**, Pan, Dierickx, Guidash, and Hashimoto disclose the device of claim 7, but do not specify that the gate electrode for read and reset of the facing light-receiving elements in the adjacent pixel rows are formed by a single electroconductive layer, and said layer is arranged to zigzag between the adjacent pixel rows.

The claim language "formed by a single electroconductive layer" describes a product by process. Product by process claims are not limited to the recitation of the steps, but only by the resulting structure. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). Ikeda teaches a delta type pixel array where the electrode lines (Fig 2A item 11n, 11m) are arranged to zigzag between adjacent pixel rows. It would have been obvious to one of ordinary skill in the art at the time of

the invention to use the teachings of Ikeda on the device of claim 7, since this electrode arrangement allows the opening (aperture) to be increased (Ikeda col 5 ln 34-35).

20. Regarding claim **13,** Pan, Dierickx, Guidash, and Joo disclose the elements as discussed with respect to claim 5.

21. With regards to claim **14**, Pan, Dierickx, Guidash, Joo and Kopley disclose the elements as discussed with respect to claim 6.

22. Regarding claim **15**, Hashimoto discloses a structure, which can perform the functional limitations of the claim (see discussion of claim 11 above).

23. With regards to claim **18**, an obvious variation of an n-channel imaging sensor is a p-channel sensor, as taught by Dierickx in claim 1 above.

24. Claims **9, 16, and 19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Pan, Guidash, and Hashimoto as applied to claim 7 above, and further in view of Joo.

25. Regarding claim **9**, Joo teaches each of the elements as discussed with respect to claim 5.

26. Regarding claim **16**, Hashimoto discloses a structure, which can perform the functional limitation of the claim (see discussion of claim 11 above).

27. With regards to claim **19**, an obvious variation of an n-channel imaging sensor is a p-channel sensor.

28. Claims **10, 17, and 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Pan, Dierickx, Guidash, Hashimoto, and Joo as applied to claim 9 above, and further in view of Kopley.

29. Regarding claim **10**, Kopley teaches each of the elements as discussed with respect to claim 6.

30. Regarding claim **17**, Hashimoto discloses a structure, which can perform the functional limitations of the claim (see discussion of claim 11 above).

31. With regards to claim **20**, an obvious variation of an n-channel imaging sensor is a p-channel sensor.

Response to Arguments

32. Applicant's arguments with respect to claims 1 and 7 have been considered but are moot in view of the new ground(s) of rejection. However, Applicant's argument that claim 1 describes a vertical transistor is not persuasive, as there is no language to that effect in the claim. The regions claimed may be met by a LDD structured photodiode as specified by Pan.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John C. Ingham whose telephone number is (571) 272-8793. The examiner can normally be reached on M-F, 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John C Ingham
Examiner
Art Unit 2814

jci